AMERICAN UNIVERSITY OF SCIENCE & TECHNOLOGY

FACULTY OF ENGINEERING
DEPARTMENT OF COMPUTER AND COMMUNICATIONS ENGINEERING

CCE 301: ELECTRONICS

Spring Term 2013-2014

Exam No.1

March 20, 2014

Student Name: ____________________ **ID Number:** ____________________

CLOSED BOOK (75 Minutes)

- The **cheating** penalty will result in a **zero**
- **Cellular Phones** are strictly prohibited in the examination hall.
- **Borrowing** of any material is not permissible.
- Write your name and ID number in the indicated space of the question booklet.
- You may use the back of any page for scratch.
- Do not detach any scratch sheet from the question booklet.
- This exam contains 12 pages (including this cover page) and 6 problems. Check to see if any pages are missing. Print your name on the top of this page, and put your initials on the top of every page, in case the pages become separated.

Problem	Points	Score
1	10	
2	10	
3	20	
4	10	
5	20	
6	30	
Total:	100	

1. (10 points) **Answer by TRUE or FALSE.**

   (a) An intrinsic semiconductor has a higher number of donors than acceptors.

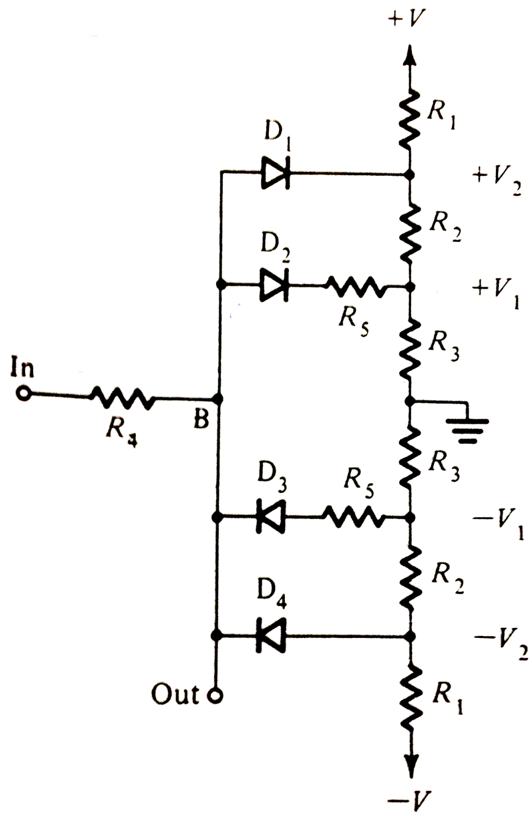
   (b) Antimony (symbol Sb from group 5 of the periodic table) would act as a donor in silicon.

   (c) When a formerly intrinsic material is converted to an extrinsic material by doping with acceptors, there are fewer electrons than when the material is intrinsic.

   (d) In equilibrium, if electron density is increased by doping, the hole density also increases to maintain charge balance.

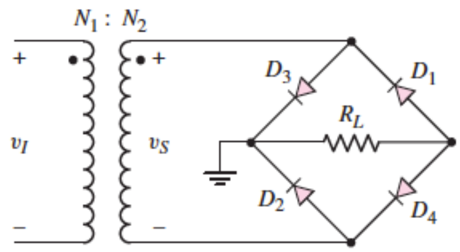
   (e) As the concentration of N-dopers increases, the barrier potential increases.

2. (10 points) **Multi-diodes circuit**
For the multi-diodes circuit shown below, assume all the diodes are ideal and all resistances are equal to 1 kΩ. The dc voltages shown, $+V$ and $-V$, each has a magnitude of 6 volts. Determine the output voltage at point B for an input voltage $v_{In} = 3V$.

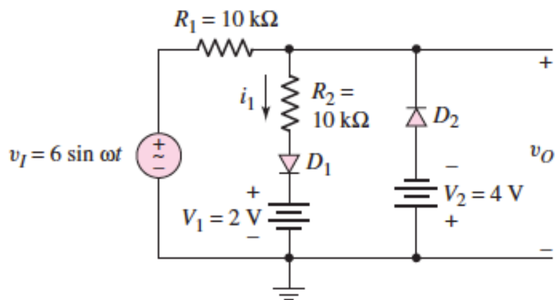


3. (20 points) **Steady State Output Voltage**

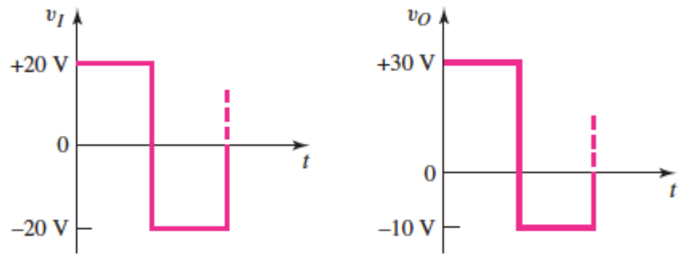
(a) Consider the following circuit, where $N_2 = 2N_1$, $v_I = 10\sin(\omega t)$, and the diodes are assumed to have a voltage drop of 0.6 V for any current. Draw the corresponding steady state output voltage across the resistor. Explain.



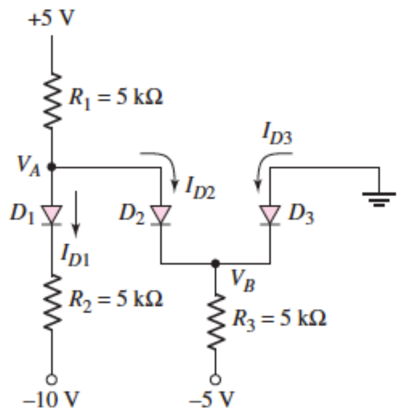
(b) Consider the following circuit, where the diodes are assumed to be ideal. Draw the corresponding steady state output voltage v_0. Explain.



4. (10 points) **Diode Clamper Design**
Design a diode clamper to generate a steady-state output voltage v_0 from the input voltage v_I in the figure below if $V_{D0} = 0$.



5. (20 points) **Diode currents and voltages.**
Determine the current in each diode and the voltages V_A and V_B in the multi-diode circuit shown below. Let $V_{D0} = 0.7V$ for each diode.



6. (30 points) **Designing a bridge rectifier.**

The objective is to design a full-wave bridge rectifier circuit with a capacitor-input filter, which operates from 100 V (rms) 60 Hz household supply through a step-down transformer having a single secondary winding. The connected load has a resistance of R kΩ, and the capacitor has a capacitance of $C\ \mu F$. We would like to satisfy the following requirements:

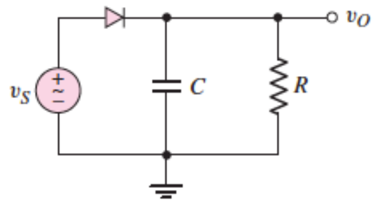
- All chosen diodes should be silicon with same potential barrier V_{D0}. (The potential barrier for a silicon diode can range from 0.6 V to 0.8 V)
- The PIV for each diode should be 19.2 V
- The peak current through the load R is measured to be 9.2 mA
- The allowed ripple voltage of the filter's output voltage is 10.95 V.

Take $\sqrt{2} = 1.4$.

(a) 1. (5 points) Precise the necessary number of windings, N, of the step-down transformer's primary leg, and the value for the potential barrier V_{D0}.
2. (5 points) Precise a value for R and C.

(b) Assume now that the capacitor is removed, and the value for $N = 5$ and $V_{D0} = 0.7V$.
1. (10 points) For what fraction of a cycle does each diode conduct?
2. (10 points) What is the average voltage across the load?

Bonus (10 points)
Consider the following circuit, which is fed by a 60 Hz sinusoid with peak value of 100 V, with a load resistance $R = 10k\Omega$ and a capacitor of capacitance $C = 83.3\mu F$. Calculate



the fraction of the cycle during which the diode is conducting.